TSMC-00-816B

October 24, 2003

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/627,013 07/25/03

Chia-Ta Hsieh et al.

A METHOD WITH TRENCH SOURCE TO INCREASE THE COUPLING OF SOURCE TO FLOATING GATE IN SPLIT GATE FLASH

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 27, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 10/27/03

U.S. Patent 6,159,801 to Hsieh et al., "Method to Increase Coupling Ratio of Source to Floating Gate in Split-Gate Flash", discloses a three-dimensional source capable of three-dimensional coupling with the floating gate of a split-gate flash memory cell.

The following two U.S. Patents propose a different split-gate flash memory cell with increased coupling ratio, and the making of the same:

1) U.S. Patent 6,017,795 to Hsieh et al., "Method of Fabricating Buried Source to Shrink Cell Dimension and Increase Coupling Ratio in Split-Gate Flash".

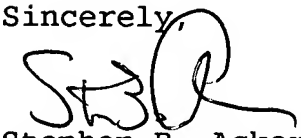
2) U.S. Patent 6,124,609 to Hsieh et al., "Split Gate Flash Memory with Buried Source to Shrink Cell Dimension and Increase Coupling Ratio".

U.S. Patent 5,527,727 to Kim, "Method of Manufacturing Split Gate EEPROM Cells", discloses a method of manufacturing a split-gate EEPROM cell where an active region is defined to include a source bit line and a drain bit line region.

U.S. Patent 6,037,221 to Lee et al., "Device and Fabricating Method of Non-Volatile Memory", describes fabrication of a non-volatile memory.

U.S. Patent 5,780,341 to Ogura, "Low Voltage EEPROM/NVRAM Transistors and Making Method", describes making of a non-volatile random access memory.

Sincerely,



Stephen B. Ackerman,
Reg.# 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OCT 2 9 2003

PATENT & TRADEMARK OFFICE

Docket Number (Optional)	Application Number
TSMC-00-816B	10/627,013
Applicant: Chia-Ta Hsieh et al.	
Filing Date: 07/25/03	Group Art Unit:

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6159801	12/12/00	Hsieh et al.	438	259	4/26/99
	5780341	7/14/98	Ogura	438	259	12/6/96
	6037221	3/14/00	Lee et al.	438	257	2/3/97
	5527727	6/18/96	Kim	437	43	9/26/95
	6124609	9/26/00	Hsieh et al.	257	315	11/15/99
	6017795	1/25/00	Hsieh et al.	438	262	5/6/98

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant